Design on CMOS Integrated Circuit of Low Power Consumption

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Keywords: low power consumption; CMOS; integrated circuit; working principles; design techniques; design methods

Abstract: An integrated circuit is a kind of microelectronic device or component. CMOS circuit is one of them. It has the advantages of high integration, low power consumption and strong anti-interference ability, and is the main technology of integrated circuits. Based on the working principle of CMOS integrated circuits, this paper analyzes the low-power CMOS integrated circuit design technology and proposes a low-power CMOS integrated circuit design method. Design techniques include: dynamic power design, static power design, and low-power synthesis. Design methods include: reduced load capacitance, sleep mode, dual threshold voltage, reduced switching activity hopping rate, asynchronous logic, input, gated clock. The research results in this paper are used to guide the practice of CMOS integrated circuit design and will play an important role in reducing CMOS integrated circuits.

1. Introduction

An integrated circuit is a miniature electronic device or component. A certain process is used to interconnect components such as transistors, resistors, capacitors, and inductors, and wirings required in a circuit, on a small or small piece of semiconductor wafer or dielectric substrate, and then packaged in a package. Inside, it becomes a micro structure with the required circuit function. All of the components of an integrated circuit is structurally integrated, making electronic components a big step toward miniaturization, low power consumption, intelligence, and high reliability. The CMOS circuit is the abbreviation of "Complementary Metal Oxide Semiconductor". It consists of an insulated field effect transistor. Because it has only one kind of carrier, it is a unipolar transistor integrated circuit. The basic structure is an N-channel MOS transistor. And a P-channel MOS transistor, because the operating voltages of the two transistors are opposite in polarity, the two gates are connected as an input terminal, and the two drains are connected as an output terminal, and the two tubes are exactly loads with each other, and are in a complementary working state The CMOS circuits have become the main technology of integrated circuits due to their high integration, low power consumption and strong anti-interference ability.

The low-power CMOS integrated circuit has the following features: First, low power consumption, FET, and complementary structure. When working, two series-connected FETs are always in one tube and the other is turned off. The state of the circuit static power is theoretically zero. Second, the anti-interference ability is strong, the typical value of the voltage noise tolerance is 45% of the power supply voltage, and the guaranteed value is 30% of the power supply voltage. Third, the input impedance is high, and the input end is generally a protection network composed of a protection diode and a series resistor, which is slightly smaller than the input resistance of a general FET. Fourth, the stability is good, the line structure and electrical parameters are symmetrical. When the temperature environment changes, some parameters can play an automatic compensation role. Fifth, the radiation resistance is strong, and various rays and radiation have limited influence on their electrical conductivity and it is especially suitable for the production of aerospace and nuclear experimental equipment. The development of the integrated circuit industry has increased the frequency and integration of CMOS circuits, and has also increased the power consumption of circuits. As process feature sizes decrease, the power consumption of the circuitry

increases exponentially. Excessive power consumption reduces the stability and reliability of the system and makes packaging difficult. Therefore, low power design is becoming an increasingly important part of current circuit design.

2. Working Principles on CMOS Integrated Circuit

Complex CMOS integrated circuits are mostly composed of inverter units. Through a basic circuit in the CMOS integrated circuit, the inverter unit analyzes its working principle. A P-channel MOS transistor and an N-channel MOS transistor are connected in a complementary manner to form a basic inverter unit, as shown in Fig .1. In the figure, Vdd is the positive power supply terminal and Vss is the negative power supply terminal. The circuit design uses a positive logic method, that is, logic "1" is high level and logic "0" is low level.

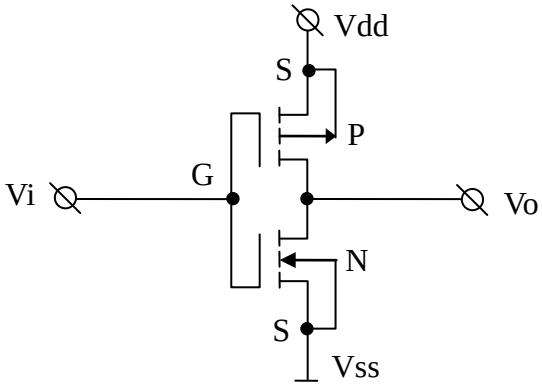

Fig.1. Inverter unit

In Fig. 1, when the input voltage Vi is low level "0" (Vss), the Gate-source voltage of the N-channel MOS transistor is VGSN = 0 V (source and substrate are connected to VSS), since it is an enhanced tube. Therefore, the tube is turned off, and the Gate-source voltage of the P-channel MOS transistor is VGSN=Vss_Vdd. If |Vss_Vdd|>|VTP| (MOS transistor turn-on voltage), the P-channel MOS transistor is turned on, so the output voltage Vo is at a high level "1" (Vdd), realizing the inversion function of the input and output.

When the input voltage Vi is low level "1" (Vdd), VGSN = (Vdd - Vss). If (Vdd—Vss)>VGSN, the N-channel MOS transistor is turned on. At this time, VGSN=0V, the P-channel MOS transistor is turned off, so the output voltage Vo is low level "0" (Vss), and Mu is mutually Inverse relationship.

It can be seen from the above analysis that when the input signal is in a steady state of "0" or "1", one of the two MOS transistors in the circuit is always in an off state, so that there is no low impedance DC path between Vdd and Vss, so static work Very little consumption.

3. Design Techniques on CMOS Integrated Circuit of Low Power Consumption

The low-power CMOS integrated circuit design technology mainly includes the following three categories:

(1) Dynamic power design. Dynamic power consumption refers to the power consumption during current operation. It mainly includes three parts: function jump power consumption caused by capacitor charge and discharge, competitive risk power caused by circuit delay, and short-circuit power consumption caused by instantaneous turn-on of the circuit. The different levels of the hardware design flow have different characteristics, and the low-power design methods are different. The main methods include the following six methods: First, the system level, some modules are closed immediately after entering the idle state, how to perform system partitioning and state prediction, Mainly through the optimization and management of power consumption. Second, the behavior level, choose a better algorithm, by optimizing the instruction structure to ensure that as few hardware as possible participate in the instruction implementation. Third, the algorithm level,

select the appropriate algorithm to reduce the hop rate, and reduce the power consumption of the circuit by reasonable division of hardware and software. Fourth, the register transfer level mainly includes gated clock, finite state code optimization, circuit balance, and bus coding. Fifth, the logic gate level is mainly to reduce the load capacitance, adjust the transistor size, select the logic device with lower power consumption, and optimize the logic structure. Sixth, the transistor stage is mainly a trade-off between power consumption, area and performance. By controlling the production process to reduce power consumption, the most typical is closed-value voltage control.

(2) Static power design. Static power consumption refers to leakage current consumption, which is the power consumption when the circuit state is stable. Static power consumption is affected by factors such as circuit structure, input state and process parameters. The main design techniques include process control method, power supply voltage control method, threshold voltage method and input vector control method. In the past, dynamic power consumption was a major part of the power consumption of the circuit. As the process progressed, the minimum line width became smaller and smaller. When the circuit process entered the deep sub-micron or deeper nano-stage, the feature size of the device became smaller and smaller. The degree is getting higher and higher, the leakage current is getting larger and larger, and as the feature size decreases, the leakage current consumption increases rapidly, and the dynamic power consumption remains basically unchanged. Therefore, the static power consumption caused by leakage current has become a non-negligible part of integrated circuit design. At present, the following technologies are mainly used: First, the threshold voltage is adjusted to control the leakage power consumption, such as using a multi-threshold voltage device, and dynamically changing the threshold voltage during operation. Second, the gated power supply technology that reduces power consumption by cutting off the power of the idle components does not generate leakage power without power supply. Third, using the cascading effect of the circuit, the input vector control technique is used for the idle components. Since the input vector affects the leakage state of the circuit, selecting a good input vector causes the circuit connected to the input to be in a low leakage state.

(3) Low-power integrated technology. Low-power synthesis technology is a further development of low-power design technology, which will reduce power consumption from the design phase to the comprehensive phase, which not only reduces the designer's pressure, but also allows the designer to put more energy into the system function design. Enhance design automation and accelerate low-power, high-performance and low-cost chip development. From the perspective of the design process, the low-power integrated technology includes high-level synthesis, system-level synthesis, and gate-level synthesis. The different levels are very different, not only making full use of the low-power technology that can be utilized at this level, but also being flexible. you can also apply more new technologies. The main purpose of low-power design is to reduce system function hopping rate, which is the main goal of low-power integrated design. High-level synthesis is a high-level description of the system, translated into a register transfer level description, mainly including two aspects of technology: low-power scheduling and register rebinding. Register transfer stages include loop unrolling, order reordering, shared operands, operator hold, and similar operation reuse. Gate-level low-power integration mainly considers clock gating, logic device selection, and data path balancing. The data path balancing is a very important factor that can greatly reduce the risk of risk.

4. Design Methods on CMOS Integrated Circuit of Low Power Consumption

Low-power CMOS integrated circuit design is a complex systemic problem. Appropriate technology must be applied in all aspects, and different methods are used to achieve the goal of reducing power consumption while maintaining system performance. Specific design methods include:

(1) Reduce the load capacitance. Load refers to the electronic components connected to the two ends of the power supply in the circuit. Load capacitance means that the two leads of the crystal are connected to the inside of the IC block and the sum of all external effective capacitors. It can be regarded as the serial connection capacitor of the crystal oscillator in the circuit. Dynamic power is

proportional to load capacitance and reducing load capacitance is an important way to reduce power consumption. In a CMOS circuit, the capacitor is mainly composed of two types. First, the device gate capacitance and the node capacitance are related to the device process. Second, the connection capacitance, the circuit should be connected to the two poles without a load. The connection is called Is a short circuit. As the process progresses, the wiring capacitance has exceeded the device capacitance. Reducing the load capacitance not only reduces the dynamic power consumption of the circuit, but also increases the operating speed of the circuit, which is an important means to reduce power consumption. In order to reduce the capacitance, a small device can be selected in the process, and the wiring length is reduced in physical design.

(2) Sleep mode. Sleep mode is an optional way to reduce power consumption. The entire system action is in the monitored state. If the system or circuit is idle for a certain period of times, and the entire system or circuit will be automatically shut down. However, the input is still in a responsive state. Once any input signal is triggered, the entire system or circuit will be reactivated and returned to normal operation, which will reduce the corresponding power consumption. This mode is longer for sleeping. The device is more advantageous. Because, from sleep state to normal working state, it sometimes takes several microseconds, even a few milliseconds; moreover, the system or circuit needs additional power consumption when it goes to sleep and returns to normal working state.

(3) Double threshold voltage. The critical path delay determines the clock speed of the synchronous circuit. However, since the number of critical paths is only a small fraction of the total number of integrated circuit paths, the gate elements on non-critical paths operate very slowly, and the performance of the circuits is not increased by the early arrival of non-critical path receiver signals. The gate unit circuit on a non-critical path consumes additional energy, causing wasted power. The dual threshold voltage technique is designed to optimize the circuit by exploiting the difference in timing delay between different signal propagation paths within the integrated circuit for non-critical path characteristics. In order to achieve the rated target clock frequency, the operating speed of the gate unit on the non-critical path is selectively reduced, and the low leakage and large delay of the high threshold voltage transistor are utilized to reduce the slack capacity of these paths and continue to be adopted on the critical path. The gate unit of the low threshold transistor maintains the delay on the path.

(4) Reduce the switch activity jump rate. The dynamic power consumption is proportional to the number of transitions between the high and low levels of the signal per unit time. You can consider reducing the power consumption of the switch to reduce the power consumption. When the signal activity is zero, even if the load capacitance is large, the circuit does not consume energy. A certain system or module of the circuit does not work. When it is in the sleep state, the clocks of these systems can be shielded, the operation and flipping of some circuits are stopped, and the power consumption of the circuit is reduced. It should be noted that the CMOS integrated circuit has a pseudo-jump, which has no effect on the circuit operation, but occupies a certain switch activity, which causes the circuit system to lose its function. In addition, the pseudo-hopping also propagates to the next-level circuit, and the more system units that pass through, the more power is consumed. Therefore, when reducing the switching activity hopping rate, it is possible to shorten the propagation length and eliminate the false hopping.

(5) Asynchronous logic. Asynchronous logic is a completely different approach to synchronous design. The maximum clock frequency of the synchronous circuit is affected by the system design process, operating environment and power supply voltage. The maximum logic delay must be met. Therefore, the high performance of the system cannot be fully utilized. Asynchronous logic does not use the global clock but uses the handshake signal circuit to coordinate the cooperation between modules, there is no clock skew problem. The gated clock is just a coarse-grained power control, which increases the clock skew problem. It must be judged and controlled in the software to turn the clock on and off. This part of the operation also generates redundant power. The single clock design makes it necessary to apply the same frequency clock to different parts of the whole chip, and some parts of the system do not need to use such high frequency, which also leads to increased power consumption. Asynchronous circuits are essentially data driven, maximizing the use of energy,

accepting modules with less data, and being able to operate at lower frequencies.

(6) Input. In the process of designing the input end, the redundant output end must be processed first, and the floating end phenomenon of the input end should be prevented to avoid destroying the logic relationship of the circuit. If the input terminal is left floating, it will result in higher input impedance and increase the interference of external noise, causing the entire circuit to malfunction and cause electrostatic breakdown. To design redundant inputs, you must use a low-level intervention. If the speed of the circuit is relatively slow, it is necessary to use the input and output terminals in parallel, and it also to intervene the long wires of the protection input. It is also necessary to control the internal inductance and the distributed capacitance to prevent damage to the internal diode due to oscillation. At the same time, it is necessary to protect the static electricity at the input end. In the process of transporting, assembling and debugging the circuit board, do grounding work to prevent electrostatic breakdown. It is also necessary to reduce the process of signal input rise and fall, avoiding large losses and preventing false triggers.

(7) Gated clock. Gated clock technology is a simple and effective power control method. The basic principle is to save current consumption by turning off functions and clocks that are not used on the chip. Among many low-power technologies, gated clocks have the strongest suppression of flip power and internal power. For a register bank, due to the flipping of the clock signal CLK, the register bank continues to read the input data temporarily during the rising of CLK. At the time, the read data is constant and consumes additional power consumption. To ensure that the register bank is not affected by the clock flip at this time, the clock input of the register bank can be turned off when the EN signal is 0, so that it is not affected by the change of the CLK terminal. This operation can be realized by the gated clock technology. When EN is 0, the register clock input ENCL remains at 0, which does not change with the flip of the source clock CLK, so the register bank does not consume additional power. To further reduce power consumption, specific gating techniques can be employed. At present, there are a wide range of multi-level gated clocks and hierarchical gated clocks. In multi-level gated clock technology, a gating unit can drive one or a group of gating units. By reducing the number of gating units by hierarchical control, combining as many register sets as possible allows the gating unit to approach the top layer, saving more power.

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